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		APPLICABLE DIVISION ■DUTY PANEL DEVELOPMENT CENTER □TFT DEVELOPMENT CENTER □LCD PRODUCTS DEVELOPMENT CENTER □EL PRODUCTION DEPT.
	SPECIFICATION	

DEVICE SPECIFICATION for

Passive Matrix COLOR LCD Module

(640×480 dots)

Model No.

LM64C35PX

□CUSTOMER'S APPROVAL

DATE

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DPK-0123

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	242.5(W)×179.4(H)×8.5MAX(D)	mm
Effective viewing Area	214.2(W)×161.4(H)	mm
Display format	640(W)×480(H) full dots	—
Dot size	0.085×RGB(W)×0.305(H)	mm
Dot spacing	0.025	mm
*1 Base color	Normally black *2	—
Weight	Approx. 390	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display
Display data "H" : ON → transmission
Display data "L" : OFF → light isolation

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 °C
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V	Ta=25 °C

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 ℃	+60 ℃	0 ℃	+40 ℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z)
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40 ℃.....95 % RH Max

Ta>40 ℃.....Absolute humidity shall be less than Ta=40 ℃/95 % RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	—	9.8 m/s²
Vibration width	0.075 mm	—
Interval	10 Hz～500 Hz～10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X/±Y/±Z

Note 4) Care should be taken so that the LCD Module may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

Table 5 Ta=25 ℃, V_{DD}=5 V±10 %

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Note 1)	3.0	3.3	5.5	V
Contrast adjust voltage	Vcon -Vss	Ta=0 ℃	0.8	—	—	V
		Ta=25 ℃	1.35	1.95	2.55	V
		Ta=40 ℃	—	—	2.80	
Input signal voltage	V_{IH}	"H" level	0.8V_{DD}	V_{DD}	V_{DD}+0.3	V
		"L" level	-0.3	V_{SS}	0.2V_{DD}	V
Input leakage current	I_{IL}	"H" level	—	—	1.0	μA
		"L" level	-1.0	—	—	μA
Supply current (Logic)	I_{DD}	Note 2)	—	160	240	mA
Rush current (Logic)	Irush	Ta=25 ℃, Power ON	3 A(pk)×25 ms+1 A(pk)×10 μs max			
Power consumption	Pd	Note 2)	—	800	1 320	mW

Note 1) Under the following conditions.;

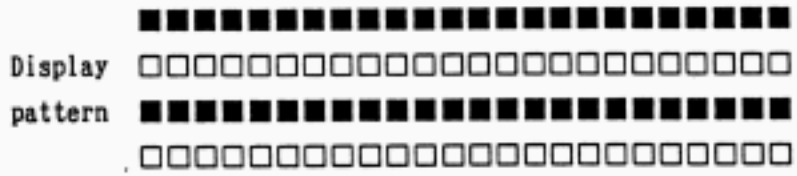
①Immediately after the rise of DISP signal. : 3 A×25 ms

②Under the situation that DISP signal is on and kept steady.: 1 A×10 μs

Note 2) Under the following conditions.;

Vcon-Vss : contrast max.(1.95 V TYP)

V_{DD}-Vss=5 V, Frame frequency=73 Hz, Display pattern = black/white stripe pattern.



This value is direct current.

5-3 Interface signals

○LCD

Table 6

Pin No	Symbol	Description	Level
1	DL4	Display data signal (Lower)	H(ON), L(OFF)
2	V_{ss}	Ground potential	–
3	DL5	Display data signal (Lower)	H(ON), L(OFF)
4	YD	Scan start-up signal	"H"
5	DL6	Display data signal (Lower)	H(ON), L(OFF)
6	LP	Input data latch signal	"H"→"L"
7	DL7	Display data signal (Lower)	H(ON), L(OFF)
8	V_{ss}	Ground potential	–
9	V_{ss}	Ground potential	
10	XCK	Data input clock signal	"H"→"L"
11	DL0	Display data signal (Lower)	H(ON), L(OFF)
12	V_{CON}	Contrast adjust voltage	–
13	DL1	Display data signal (Lower)	H(ON), L(OFF)
14	V_{DD}	Power supply for logic and LCD (+5V)	–
15	V_{ss}	Ground potential	–
16	V_{DD}	Power supply for logic and LCD (+5V)	–
17	DL2	Display data signal (Lower)	H(ON), L(OFF)
18	DISP	Display control signal	H(ON), L(OFF)
19	DL3	Display data signal (Lower)	H(ON), L(OFF)
20	NC	–	–
21	V_{ss}	Ground potential	–
22	DU3	Display data signal (Upper)	H(ON), L(OFF)
23	DU4	Display data signal (Upper)	H(ON), L(OFF)
24	DU2	Display data signal (Upper)	H(ON), L(OFF)
25	DU5	Display data signal (Upper)	H(ON), L(OFF)
26	DU1	Display data signal (Upper)	H(ON), L(OFF)
27	V_{ss}	Ground potential	–
28	DU0	Display data signal (Upper)	H(ON), L(OFF)
29	DU6	Display data signal (Upper)	H(ON), L(OFF)
30	V_{ss}	Ground potential	–
31	DU7	Display data signal (Upper)	H(ON), L(OFF)

○CCFT

Pin No	Symbol	Description	Level
1	HV	High voltage lineal (from Inverter)	–
2	NC		–
3	GND	Ground line (from Inverter)	–

NOTE) Pin No. and its location are shown in Fig.10.

○LCD

Used connector:DF9B-31P-1V (HIROSE)

Mating connector:DF9B-31S-1V (HIROSE)

○CCFT

Used connector:BHR-03VS-1 (JST)

Mating connector:SM03(4.0)B-BHS or SM02(8.0)B-BHS (JST)

Except above connector shall be out of guaranty

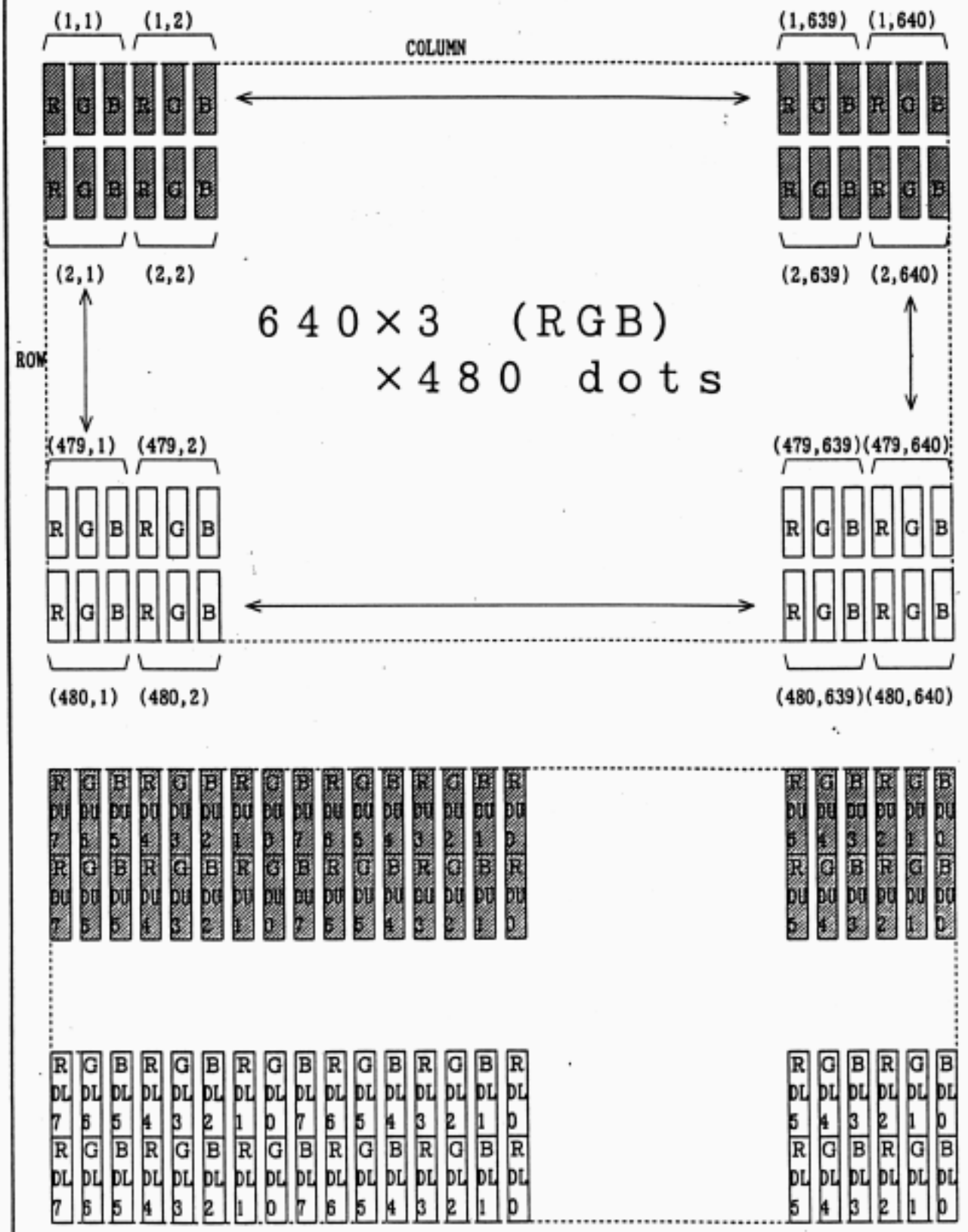


Fig.1 Dot chart of display area

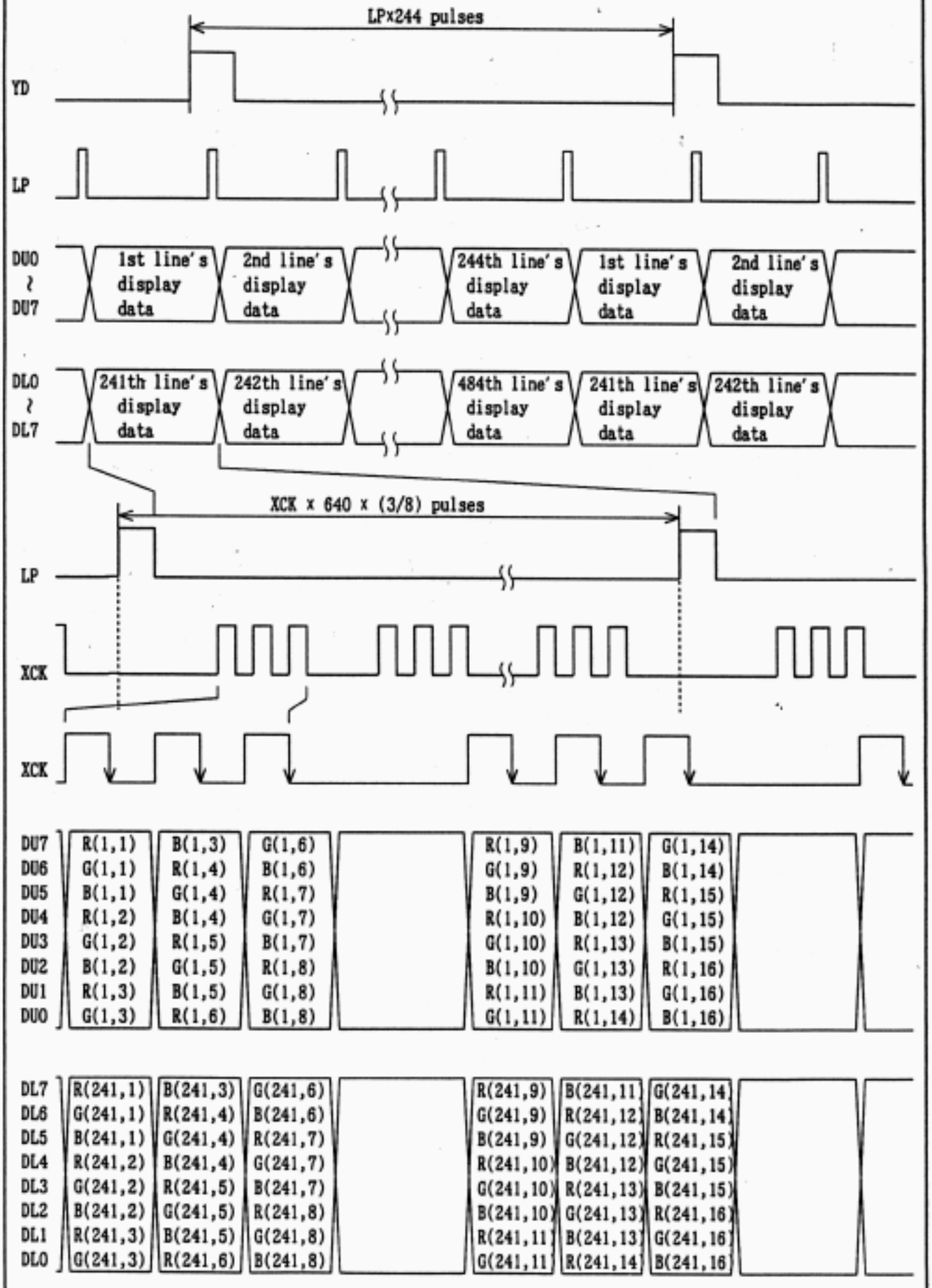


Fig.2 Data input timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating MIN.	Rating TYP.	Rating MAX.	Unit
Frame cycle *1	tFRM	8.33		16.94	ms
YD signal "H" level set up time	tHYS	100			ns
"H" level hold time	tHYH	100			ns
"L" level set up time	tLYS	100			ns
"L" level hold time	tLYH	40			ns
LP signal "H" level pulse width	tWLPH	200			ns
XCK signal clock cycle	tCK	82			ns
"H" level clock width	tWCKH	30			ns
"L" level clock width	tWCKL	30			ns
Data set up time	tDS	30			ns
hold time	tDH	30			ns
LP↑ allowance time from XCK↓	tLS	200			ns
XCK↑ allowance time from LP↓	tLH	200			ns
Input signal rise/fall time	tr,tf			13	ns

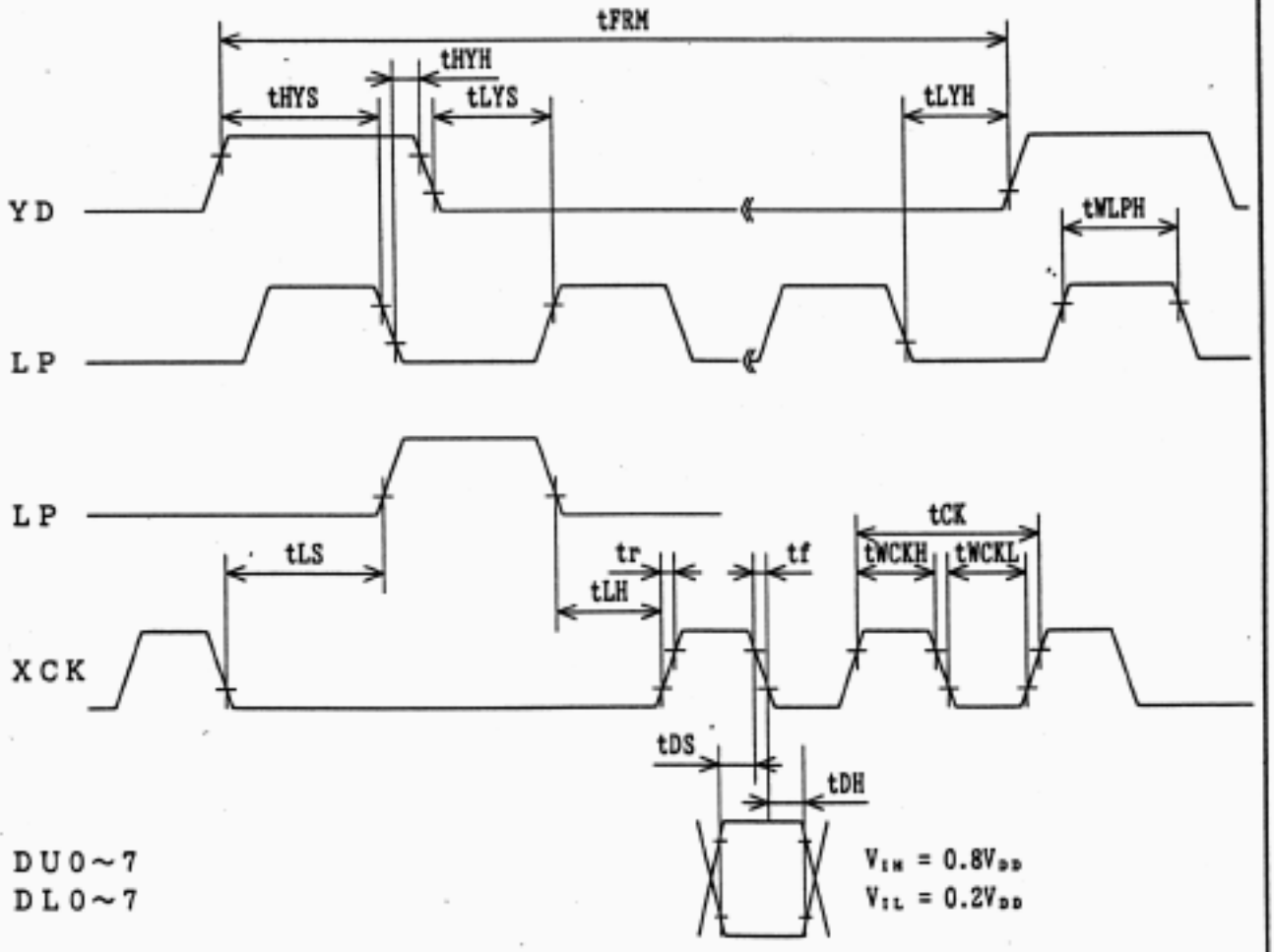


Fig.3 Interface timing chart

*1 LCD module functions at the minimum frame cycle of 8.33 ms(Maximum frame frequency of 120 Hz).
Owing to the characteristics of LCD module,"shadowing" will become more eminent as frame frequency goes up,while flicker will be reduced.

According to our experiments,frame cycle of 12.8 ms Min. or frame frequency of 78 Hz Max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgement of display quality is subjective and display quality such as "shadowing" is pattern dependent,it is recommended that decision of frame frequency, to which power consumption of the LCD module is proportional,be made based on your own through testing on the LCD module with every possible patterns displayed on it.

※ The intervals of one LP fall and the next must be always the same, and LPs must be input continuously.
The interval must be 70 μs Max.

6. Module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the Module's circuitry.

6.2 Display Face Configuration

The display consists of 640×3 (R,G,B)×480 dots as shown in Fig.1.
The interface is single panel with double drive to be driven at 1/244 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (640×3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal(XCK).

When input of one row (640 x 3,R,G,B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 640 x 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640×3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 244th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.
Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DU0~7 and DL0~7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.